Dual Complementary MOSFET

- **N Channl**

  30V/60A

  $R_{DS(ON)}$=6mΩ (typ) @VGS=10V

  $R_{DS(ON)}$=8mΩ (typ) @VGS=4.5V

- **P Channl**

  -30V/-50A

  $R_{DS(ON)}$=13mΩ (typ) @VGS=10V

  $R_{DS(ON)}$=18mΩ (typ) @VGS=4.5V

- 100% UIS & RG Tested

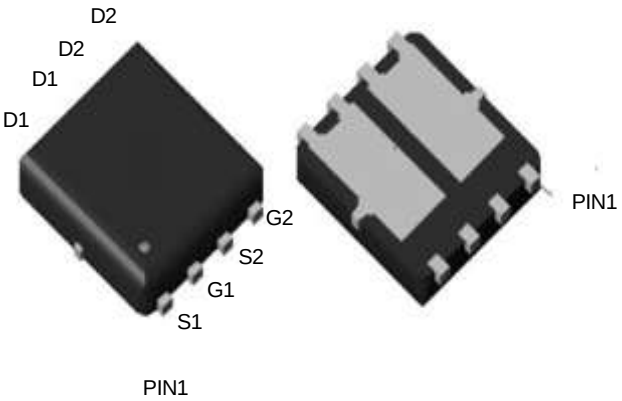
- Reliableand Rugged

- Lead Freeand Green Devices Available
  (RoHS Compliant)

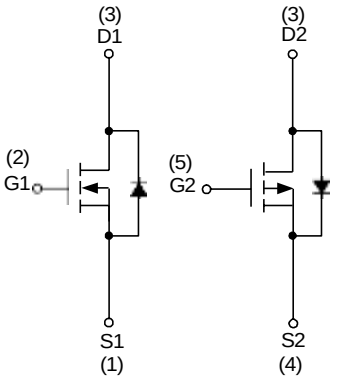
Applications

- Power Management for Industrial DC/DC
  Converters

Pin Description



PDFN5X6_8L_EP2



N-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A= 25°C unless otherwise noted)

Symbol	Parameter		N Channl	P Channl	Unit
Common Ratings					
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		±20	±20	
I_D	Continuous Drain Current G	Tc=25°C	70	-50	A
		Tc=100°C	30	-20	
I_{DM}	Pulsed Drain Current C		90	-75	A
I_{DSM}	Pulsed Drain Current	T_A=25°C	13	11	
		T_A=70°C	15	-9	
I_S	Diode Continuous Forward Current		15	-10	A
T_j	Maximum Junction Temperature		150		°C
T_{STG}	Storage Temperature Range		-55 to 150		
P_D	Maximum Power Dissipation B	T_C=25°C	40	30	W
		T_C=100°C	20	14	
P_{DSM}	Power Dissipation A	T_A=25°C	15	10	W
		T_A=70°C	10	7	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	t≤10S	45	40	°C/W
		Steady State C	80	65	
$R_{\theta JC}$	Thermal Resistance-Junction to Case		15	8	°C/W
E_{AS}	Single pulsed avalanlce energy C	L=0.1mH	210	150	Mj
I_{AS}	Single pulsed avalanlce Current C		29	-20	A

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

N-Channl Electrical Characteristics (T_J= 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	N-Channl			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =24V, V_{GS}=0V	-	-	1	μA
		T_j=55°C	-	-	5	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_{DS}=250μA	1	1.2	2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=7A		6	7	mΩ
		V_{GS}=4.5V, I_{DS}=5A		8	9	
Body Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD}=1A, V_{GS}=0V	-	0.75	1	V
g_{FS}	Forward Transconductance	V_{DS}=5V,I_D=10A	-	43	-	S
t_{rr}	Reverse Recovery Time	I_{DS}=10A, dI_{SD}/dt=500A/μs	-	7	-	ns
Qrr	Reverse Recovery Charge		-	8	-	nC
Dynamic Characteristics[e]						
R_G	Gate Resistance	F=1MHz, V_{GS}=0V, V_{DS}=0V	0.8	1.6	2.4	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS} =15V, Frequency=1.0MHz	-	760	-	pF
C_{oss}	Output Capacitance		-	125	-	
C_{rss}	Reverse transfer capacitance		-	70	-	
$t_{d(ON)}$	Turn-on delay Time	V_{GEN}=10V ,V_{DD}=15V R_G=3Ω, RL=1.25Ω	-	4.4	-	nS
t_r	Turn-on rise Time		-	9	-	
$t_{d(OFF)}$	Turn-off delay Time		-	17	-	
t_f	Turn-off rise Time		-	6	-	
Gate Charge Characteristics[e]						
Q_g	Total Gate Charge (10V)	V_{DS} =15V, V_{GS}=10V, I_{DS}=10A	-	14	20	nC
Q_g	Total Gate Charge (4.5V)		-	6.6	10	
Q_{gs}	Gate-Source Charge		-	2.4	-	
Q_{gd}	Gate-Drain Charge		-	3	-	

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

N-CHANNL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

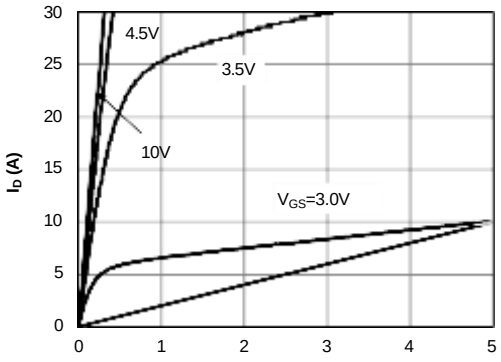


Figure 1: On-Region Characteristics (Note E)

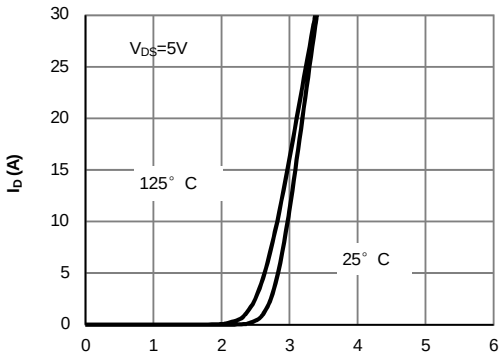


Figure 2: Transfer Characteristics (Note E)

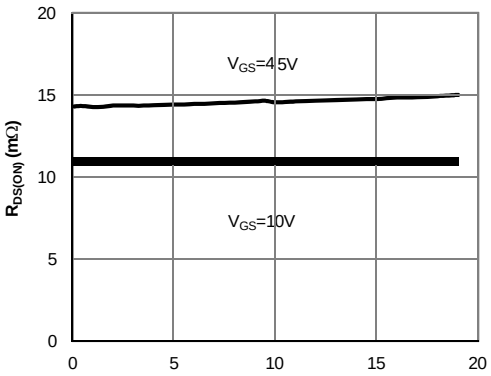


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

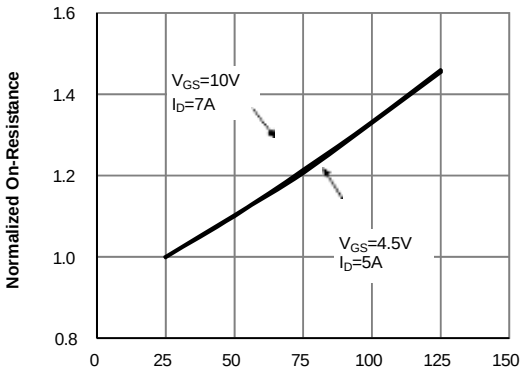


Figure 4: On-Resistance vs. Junction Temperature (Note E)

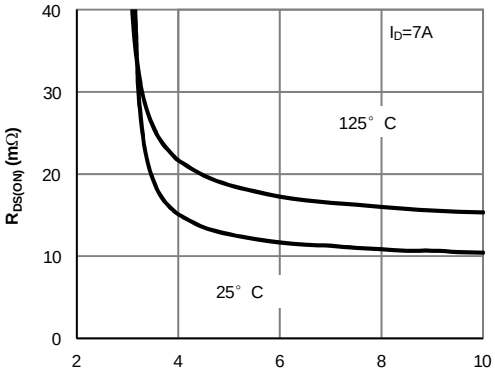


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

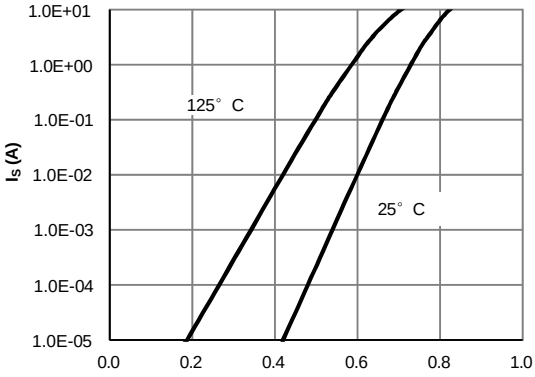


Figure 6: Body-Diode Characteristics (Note E)

N-CHANNL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

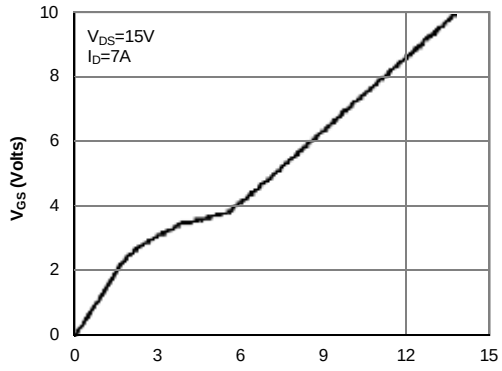


Figure 7: Gate-Charge Characteristics

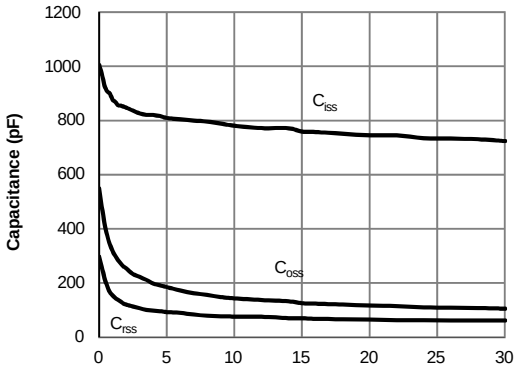
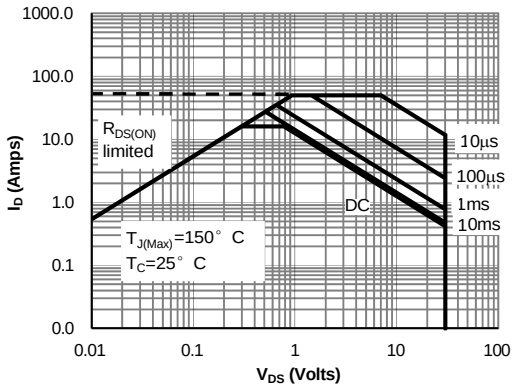


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

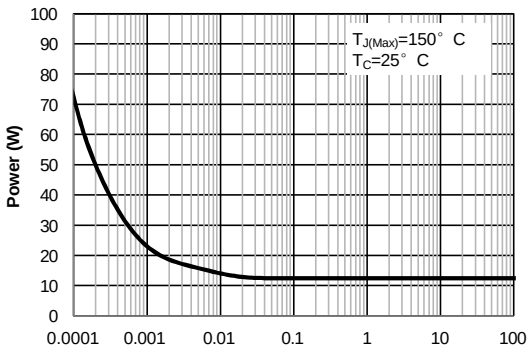


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

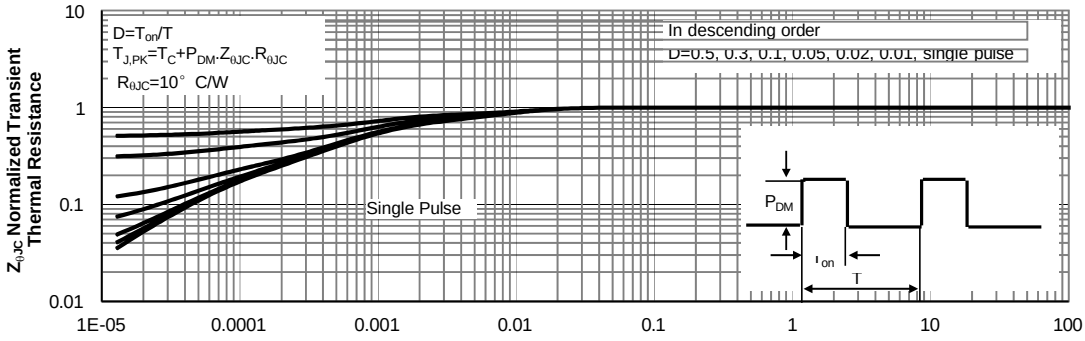


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-CHANNL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

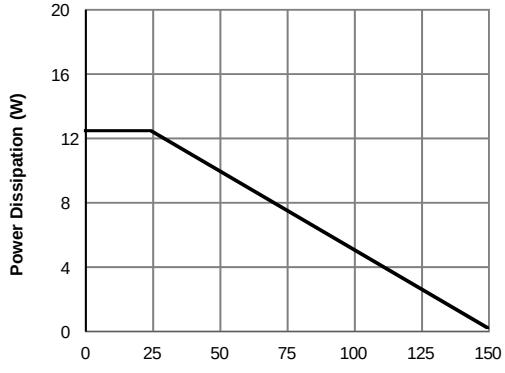


Figure 12: Power De-rating (Note F)

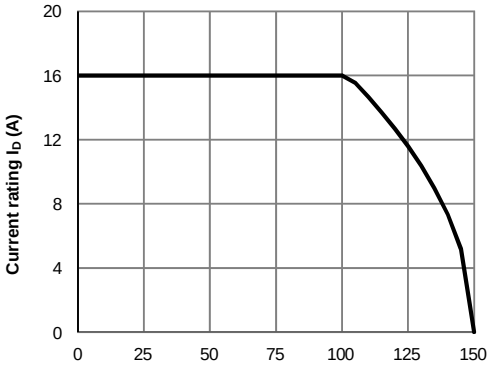


Figure 13: Current De-rating (Note F)

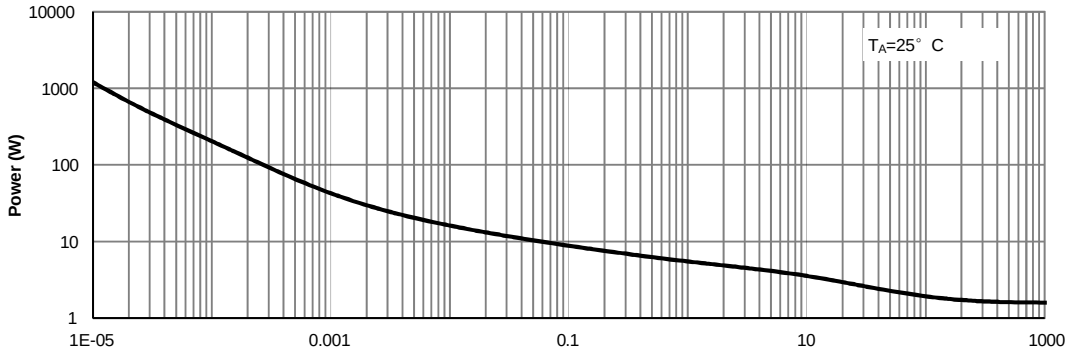


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

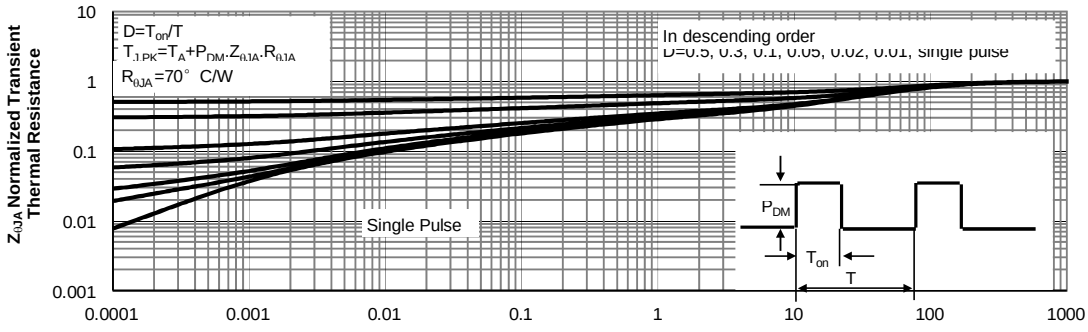


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

P-Channl Electrical Characteristics (T_J= 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	P-Channl			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250A	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-24V, V_{GS}=0V	-	-	-1	μA
		T_j=55°C	-	-	-5	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_{DS}=-250A	-1	-1.4	-2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=-10V, I_{DS}=-6A		13	14.5	mΩ
		V_{GS}=-4.5V, I_{DS}=-5A		14.5	19	
Body Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD}=-1A, V_{GS}=0V	-	-0.75	-1.0	V
g_{FS}	Forward Transconductance	V_{DS}=-5V,I_D=-6A		27		S
t_{rr}	Reverse Recovery Time	I_{DS}=-6A, dI_{SD}/dt=500A/μs	-	11.5	-	ns
Qrr	Reverse Recovery Charge		-	25	-	nC
Dynamic Characteristics[e]						
R_G	Gate Resistance	F=1MHz, V_{GS}=0V,V_{DS}=0V	2	4	6	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, Frequency=1.0MHz	-	1040	-	pF
C_{oss}	Output Capacitance		-	180	-	
C_{rss}	Reverse transfer capacitance		-	125	-	
$t_{d(ON)}$	Turn-on delay Time	V_{GEN}=-10V ,V_{DD}=-15V R_G=3Ω, R_L=1.5Ω	-	10	-	nS
t_r	Turn-on rise Time		-	5.5	-	
$t_{d(OFF)}$	Turn-off delay Time		-	26	-	
t_f	Turn-off rise Time		-	9	-	
Gate Charge Characteristics[e]						
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_{DS}=-6A	-	19	30	nC
Q_g	Total Gate Charge		-	9.6	15	
Q_{gs}	Gate-Source Charge		-	3.6	-	
Q_{gd}	Gate-Drain Charge		-	4.6	-	

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C.

P-CHANNL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

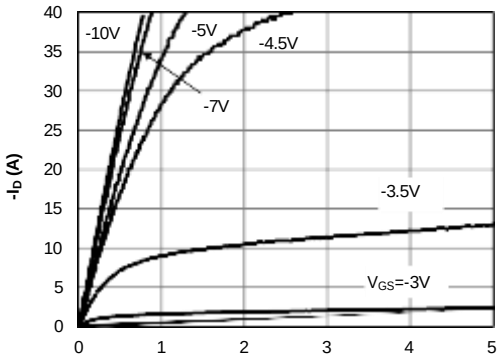


Figure 1: On-Region Characteristics (Note E)

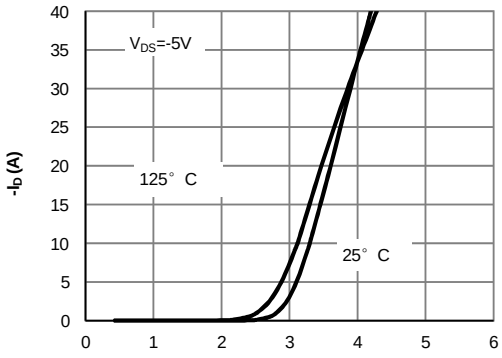


Figure 2: Transfer Characteristics (Note E)

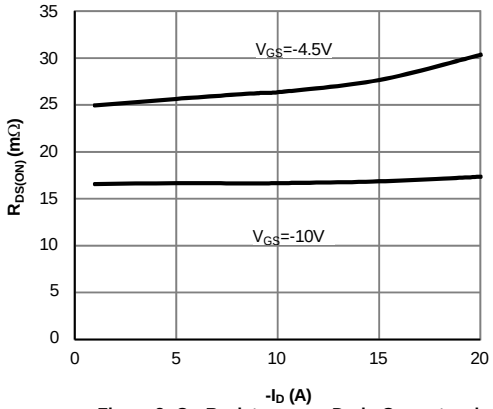


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

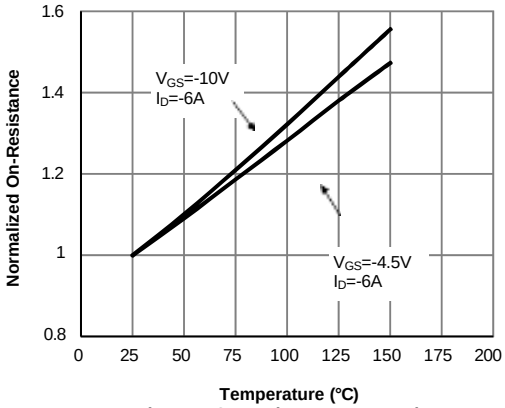


Figure 4: On-Resistance vs. Junction Temperature (Note E)

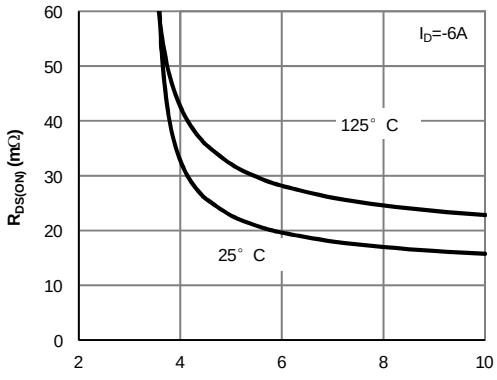


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

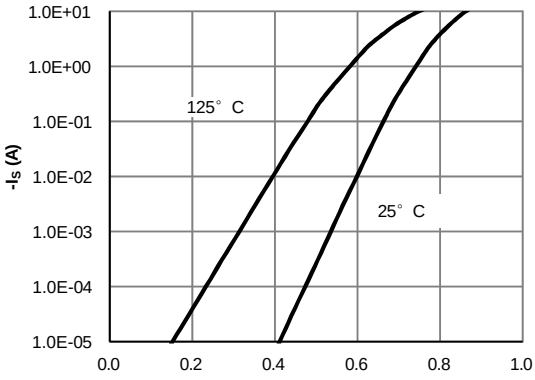


Figure 6: Body-Diode Characteristics (Note E)

P-CHANNL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

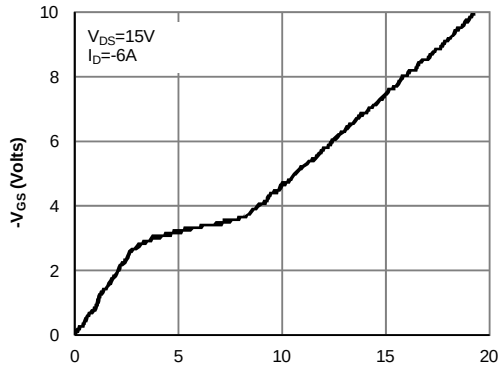


Figure 7: Gate-Charge Characteristics

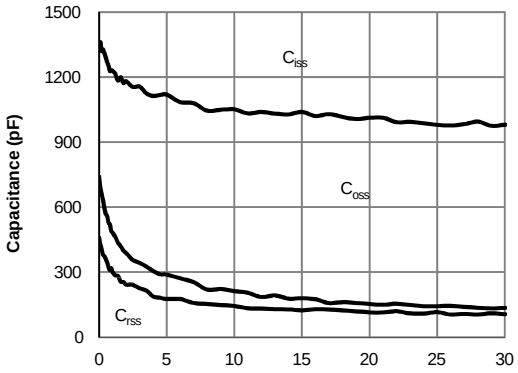


Figure 8: Capacitance Characteristics

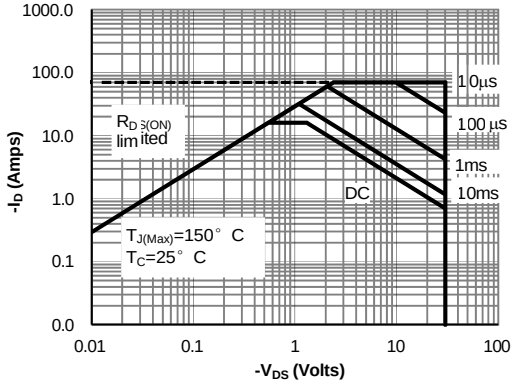


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

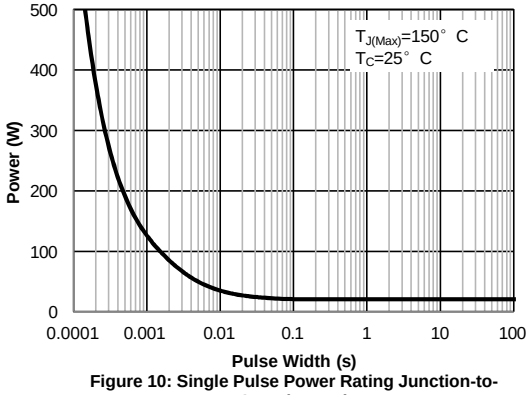


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

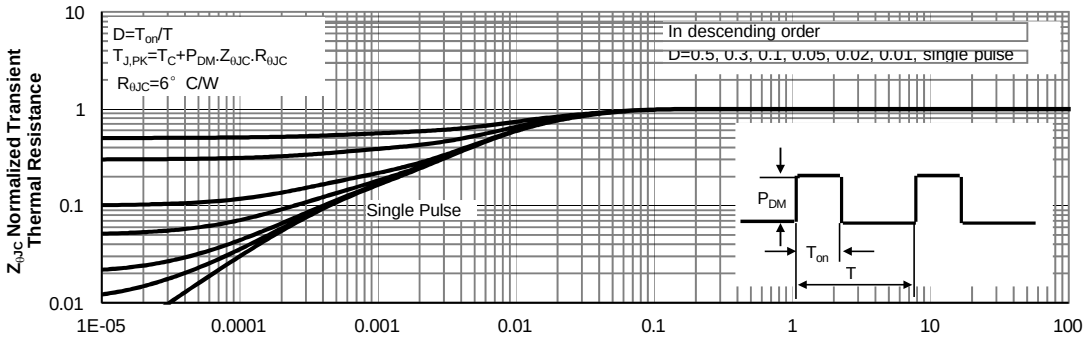


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

P-CHANNL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

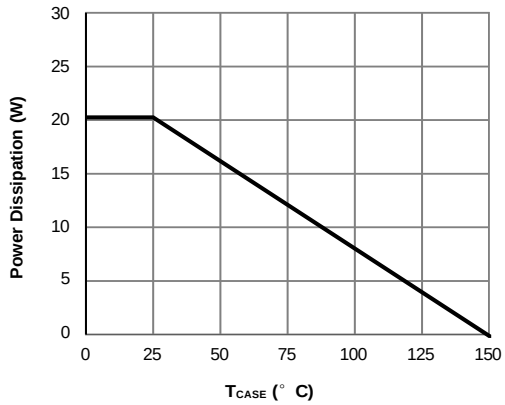


Figure 12: Power De-rating (Note F)

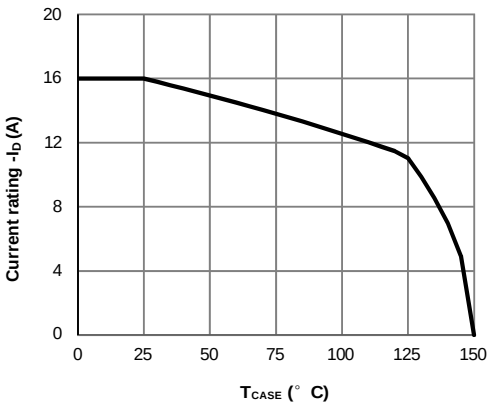


Figure 13: Current De-rating (Note F)

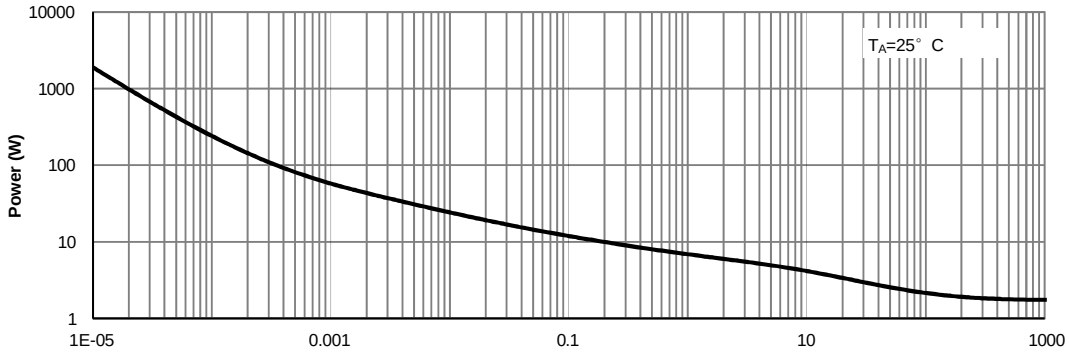


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

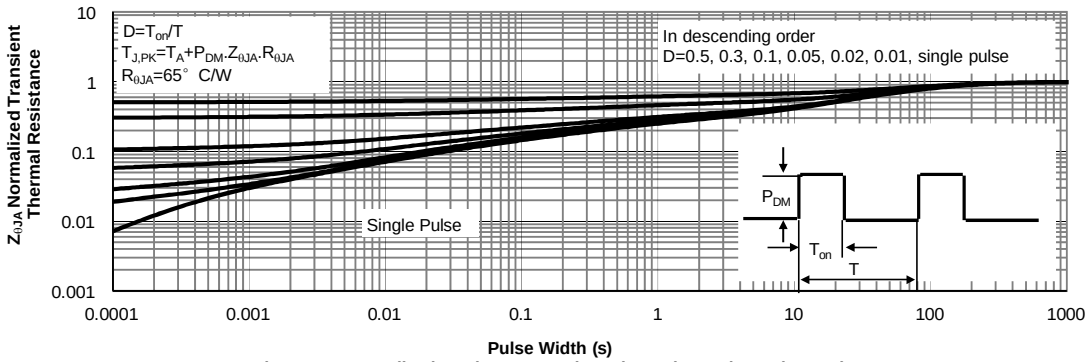


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

Gate Charge Test Circuit & Waveforms

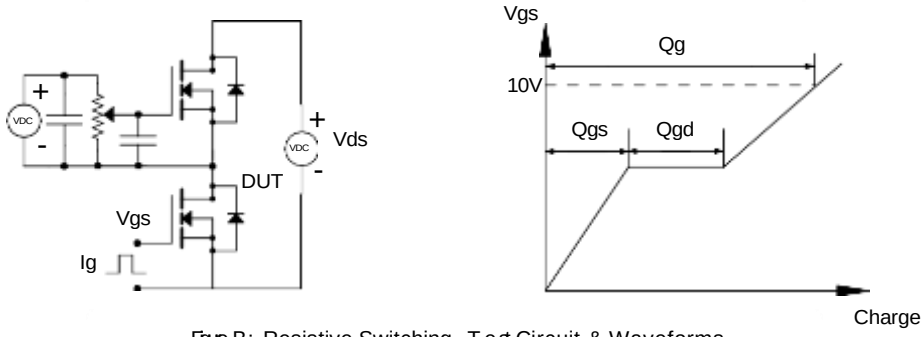


Figure B: Resistive Switching Test Circuit & Waveforms

Resistive Switching Test Circuit & Waveforms

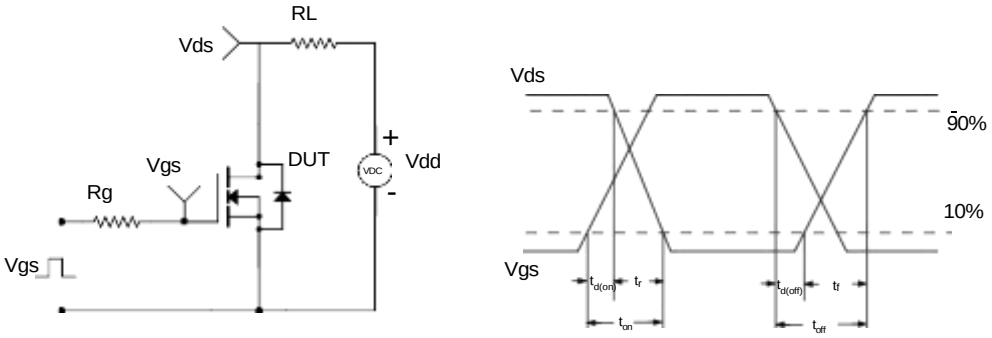


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

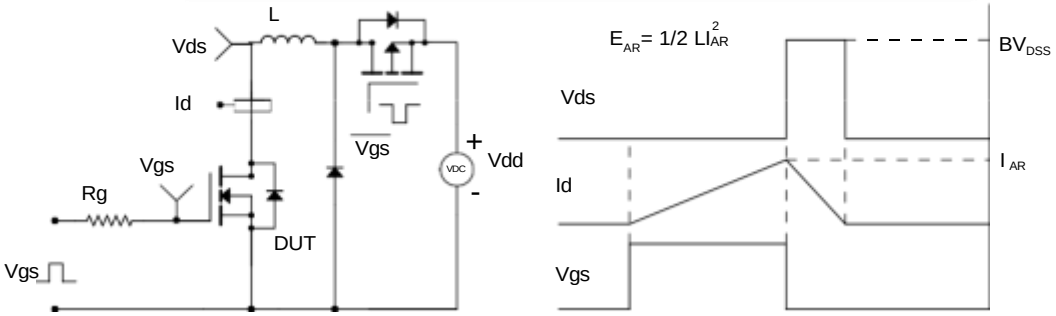
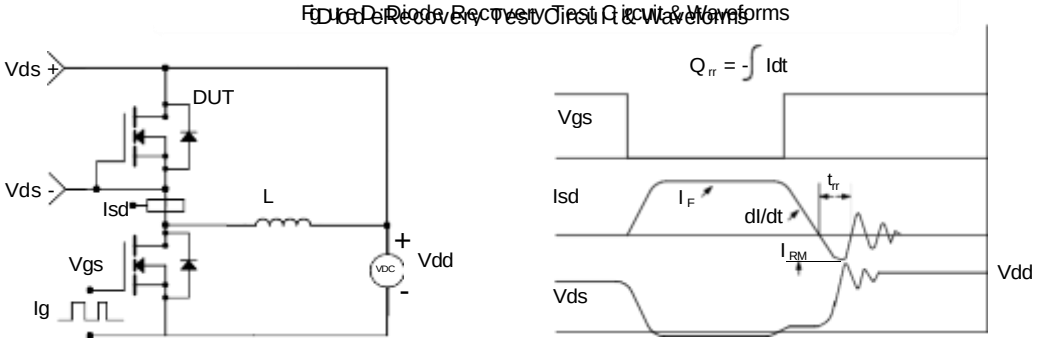
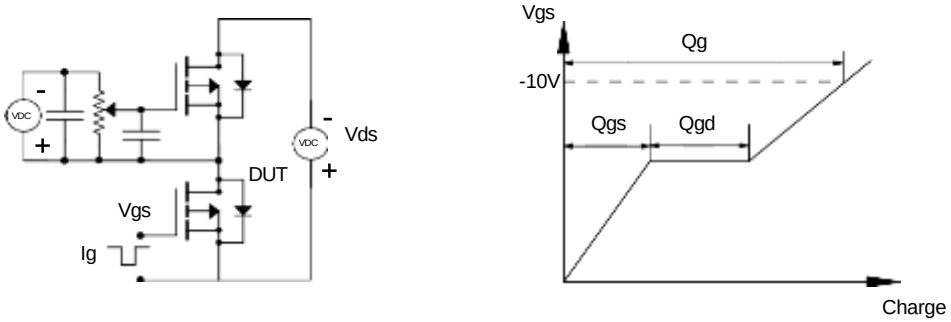


Figure D: Diode Recovery Test Circuit & Waveforms

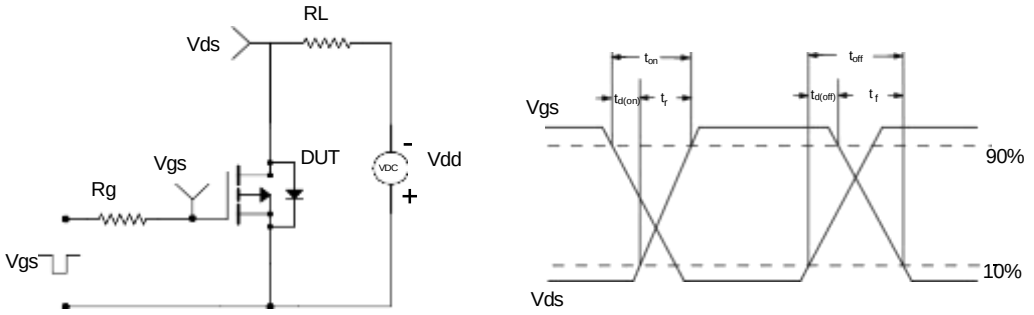
Diode Recovery Test Circuit & Waveforms



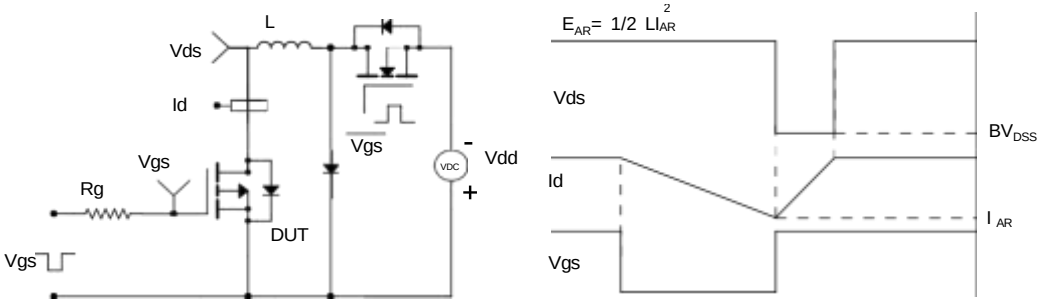
Gate Charge Test Circuit & Waveform



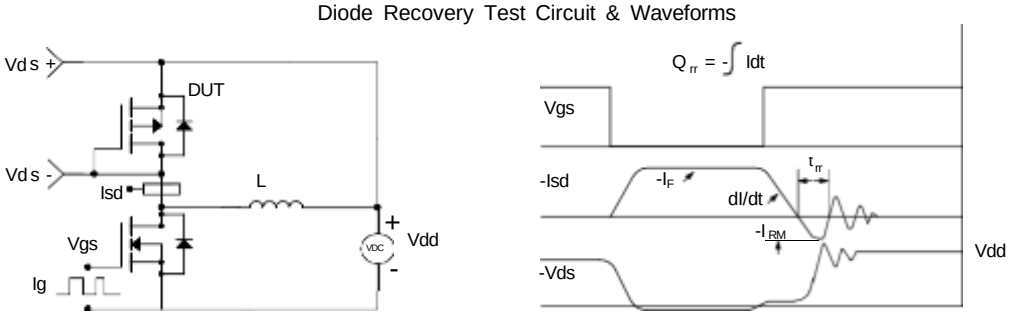
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



PDFN5×6 OUTLINE