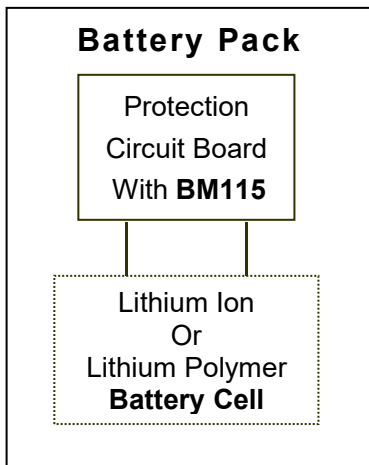


One-Cell Li Battery Protectors

General Description

The BM115-VFAA-DE is protector for lithium-ion and lithium polymer rechargeable battery with high accuracy voltage detection. It can be used for protecting single cell lithium-ion or/and lithium polymer battery packs from overcharge, overdischarge over current and short circuit. The IC has suitable protection delay functions and low power consumption property.

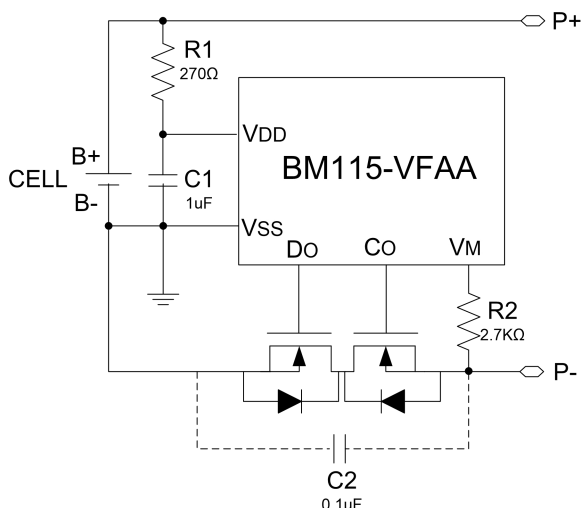
Applications



Features

- **Overcharge Detection voltage**
 - 4.425V
 - Accuracy $\pm 20\text{mV}$ (25°C)
 - $\pm 50\text{mV}$ (-40°C~85°C)
- **Overdischarge Detection voltage**
 - 2.900V
 - Accuracy $\pm 50\text{mV}$
- **Discharge Overcurrent Detection voltage**
 - 0.050V @ $V_{DD} = 3.800\text{V}$
 - Accuracy $\pm 5\text{mV}$
- **Short Circuit Detection voltage**
 - Typ. 0.100V @ $V_{DD} = 3.800\text{V}$
 - Accuracy $\pm 40\text{mV}$
- **Low Supply Current**
 - Typ. 2.5uA @ $V_{DD} = 3.400\text{V}$ (Standard Working)
 - Typ. 0.1uA @ $V_{DD} = 1.500\text{V}$ (Without auto wake up)
- **Small Package**
 - DFN 1.6*1.9-6L

Typical Application Circuits



Notes

R₁ and C₁ are to stabilize the supply voltage of the BM115-VFAA-DE. R₁ C₁ is hence regarded as the time constant for V_{DD} pin. R₁ and R₂ can also be a part of current limit circuit for the BM115-VFAA-DE. Recommended values of these elements are as follows:

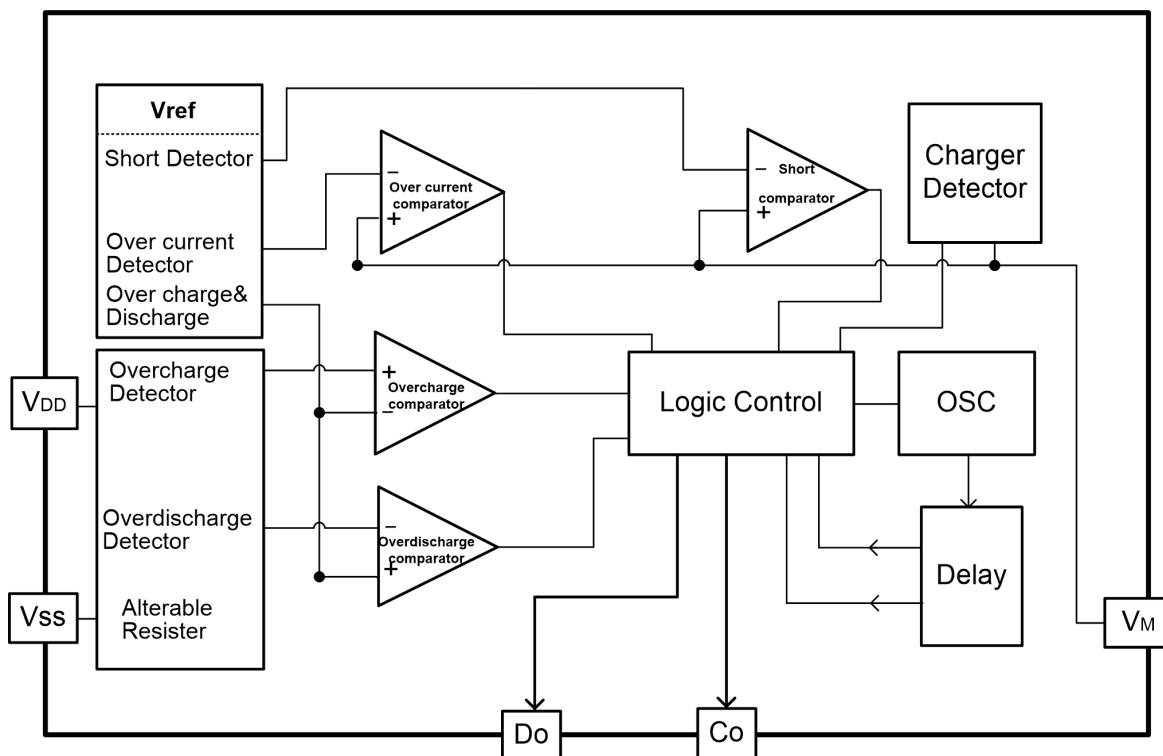
- 200Ω < R₁ < 400Ω. A larger value of R₁ results in higher detection voltage, introducing errors.
- 2kΩ < R₂ < 4KΩ. A larger value of R₂ possibly prevents resetting from over-discharge even with a charger.
- R₁ + R₂ > 2.5KΩ. Smaller values may lead to power consumption over the maximum dissipation rating of the BM115-VFAA-DE.

The requirement or resistors and capacitors and the value of constants should be decided depending upon the system function and characteristics.

Marking contents

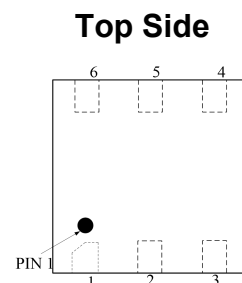
Symbol	Meaning	Top View
VFAA	Product Name	
YW	Lot Number	

Block Diagram



Pin Description

Pin	Symbol	Description
1	NC	No connection
2	Co	FET gate connection pin for charge control, CMOS output
3	Do	FET gate connection pin for discharge control, CMOS output
4	VSS	Ground
5	VDD	Power supply
6	VM	Voltage detection pin between VM and VSS, Overcurrent detection



**Electrical****Characteristics**

(Ta=25°C unless otherwise specified)

Symbol	Item	Conditions	Min.	TYP.	Max.	Unit
DETECTION VOLTAGE AND DELAY TIME						
Vdet1	Overcharge Detection Voltage	-	4.405	4.425	4.445	V
Vrel1	Release Voltage For Overcharge Detection	-	4.175	4.225	4.275	V
Vdet2	Overdischarge Detection Voltage	-	2.850	2.900	2.950	V
Vrel2	Release Voltage For Overdischarge	-	2.900	3.000	3.100	V
Vdet3	Discharge Overcurrent Detection Voltage	V _{DD} = 3.800V	0.045	0.050	0.055	V
Vshort	Short Protection Voltage	V _{DD} = 3.800V	0.060	0.100	0.140	V
Vcha	Charger Detection (Charge Overcurrent)	-	-0.055	-0.050	-0.045	V
V0cha	0V Battery Charge Starting Charger Voltage	Applied for 0V battery charge function	1.2	-	-	V
Tvdet1	Overcharge Detection Delay Time	V _{DD} = 4.0V→4.5V	700	1000	1300	ms
Tvrel1	Overcharge Release Delay Time	V _{DD} = 4.5V→4.0V	9	16	30	ms
Treset	Overcharge Reset Delay Time	V _{DD} = 4.5V→4.0V→4.5V	7	14	28	ms
Tvdet2	Overdischarge Detection Delay Time	V _{DD} = 4.0V→2.0V	44.8	64	83.2	ms
Tvrel2	Overdischarge Release Delay Time	V _{DD} = 2.0V→3.0V, V _M = 0V	1.4	2.0	2.6	ms
Tvdet3	Discharge Overcurrent Detection Delay Time	V _{DD} = 3.8V, V _M = 0V→0.2V	11.2	16	20.8	ms
Tab	Charge Overcurrent Detection Delay Time	V _{DD} = 3.8V, V _M = 0V→0.2V	5.6	8	10.4	ms
Tshort	Short Detection Delay Time	V _{DD} = 3.8V, V _M = 0V→1.2V	262.5	375	487.5	us
Tvrel3	Discharge Overcurrent Release Delay Time	V _{DD} = 3.8V, V _M = 0.2V→0 V	1.4	2.0	2.6	ms
Vriov	Discharge Overcurrent Release Voltage	-	0.70* V _{DD}	0.80* V_{DD}	0.95* V _{DD}	V
OUTPUT VOLTAGE AND V_M INTERNAL RESISTANCE						
V _{COL}	CO Pin L Voltage	I _{OL} =50uA, V _{DD} =4.5V	0.15	0.20	0.25	V
V _{COH}	CO Pin H Voltage	I _{OH} =-50uA, V _{DD} =3.9V	3.65	3.70	3.75	V
V _{DOL}	DO Pin L Voltage	I _{OL} =50uA, V _{DD} =2.0V	0.05	0.07	0.09	V
V _{DOH}	DO Pin H Voltage	I _{OH} =-50uA, V _{DD} =3.9V	3.81	3.83	3.85	V
R _{VMD}	Resistance between V _M and V _{DD}	V _{DD} =2.0V, V _M =0V	400	800	1600	kΩ
R _{VMS}	Resistance between V _M and V _{SS}	V _{DD} =3.3V, V _M =1V	10	20	40	kΩ
OPERATION VOLTAGE AND CURRENT CONSUMPTION						
V _{DD}	Operating Input Voltage	V _{DD} -V _{SS}	1.6	V_{DD}	8	V
V _M	Operating Input Voltage	V _{DD} -V _M	1.5	-	28	V
I _{DD}	Supply Current	V _{DD} = 3.4V, V _M = 0V	-	2.5	5.0	uA
I _{STANDBY}	Standby Current (without Auto wake up)	V _{DD} = 1.5V, V _M = 0V→1.5V	-	0.1	0.5	uA

**Electrical Characteristics** ^{1*}

(Ta = -40°C~85°C unless otherwise specified)

Symbol	Item	Conditions	Min.	TYP.	Max.	Unit
DETECTION VOLTAGE AND DELAY TIME						
Vdet1	Overcharge Detection Voltage	-	4.375	4.425	4.475	V
Vrel1	Release Voltage For Overcharge Detection	-	4.160	4.225	4.290	V
Vdet2	Overdischarge Detection Voltage	-	2.800	2.900	3.000	V
Vrel2	Release Voltage For Overdischarge	-	2.900	3.000	3.100	V
Vdet3	Discharge Overcurrent Detection Voltage	V _{DD} = 3.800V	0.040	0.050	0.060	V
Vshort	Short Protection Voltage	V _{DD} = 3.800V	0.050	0.100	0.150	V
Vcha	Charger Detection (Charge Overcurrent)	-	-0.060	-0.050	-0.040	V
V0cha	0V Battery Charge Starting Charger Voltage	Applied for 0V battery charge function	1.2	-	-	V
Tvdet1	Overcharge Detection Delay Time	V _{DD} = 4.0V→4.5V	500	1000	1500	ms
Tvrel1	Overcharge Release Delay Time	V _{DD} = 4.5V→4.0V	8	16	31	ms
Treset	Overcharge Reset Delay Time	V _{DD} = 4.5V→4.0V→4.5V	6	14	29	ms
Tvdet2	Overdischarge Detection Delay Time	V _{DD} = 4.0V→2.0V	32	64	96	ms
Tvrel2	Overdischarge Release Delay Time	V _{DD} = 2.0V→3.0V, V _M = 0V	1	2	3	ms
Tvdet3	Discharge Overcurrent Detection Delay Time	V _{DD} = 3.8V, V _M = 0V→0.2V	8	16	24	ms
Tab	Charge Overcurrent Detection Delay Time	V _{DD} = 3.8V, V _M = 0V→0.2V	4	8	12	ms
Tshort	Short Detection Delay Time	V _{DD} = 3.8V, V _M = 0V→1.2V	187.5	375	600	us
Tvrel3	Discharge Overcurrent Release Delay Time	V _{DD} = 3.8V, V _M = 0.2V→0 V	1	2	3	ms
Vriov	Discharge Overcurrent Release Voltage	-	0.70* V _{DD}	0.80* V_{DD}	0.95* V _{DD}	V
OUTPUT VOLTAGE AND V_M INTERNAL RESISTANCE						
V _{COL}	CO Pin L Voltage	I _{OL} =50uA, V _{DD} =4.4V	0.05	0.2	0.35	V
V _{COH}	CO Pin H Voltage	I _{OH} =-50uA, V _{DD} =3.9V	3.55	3.7	3.85	V
V _{DOL}	DO Pin L Voltage	I _{OL} =50uA, V _{DD} =2.0V	0.03	0.07	0.11	V
V _{DOH}	DO Pin H Voltage	I _{OH} =-50uA, V _{DD} =3.9V	3.79	3.83	3.87	V
R _{VMD}	Resistance Between V _M And V _{DD}	V _{DD} =2.0V, V _M = 0V	200	800	3000	kΩ
R _{VMS}	Resistance Between V _M And V _{SS}	V _{DD} =3.3V, V _M =1V	5	20	50	kΩ
OPERATION VOLTAGE AND CURRENT CONSUMPTION						
V _{DD}	Operating Input Voltage	V _{DD} -V _{SS}	1.6	V_{DD}	8	V
V _M	Operating Input Voltage	V _{DD} -V _M	1.5	-	28	V
I _{DD}	Supply Current	V _{DD} = 3.4V, V _M = 0V	-	2.5	5.5	uA
I _{STANDBY}	Standby Current (without Auto wake up)	V _{DD} = 1.5V, V _M = 0V→1.5V	-	0.1	1.0	uA

1* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.

**Absolute Maximum Ratings** ($T_a=25^{\circ}\text{C}$ $V_{SS}=0\text{V}$)

Symbol	Item	Ratings	Unit
V_{DD}	Supply Voltage	-0.3 to 8	V
V_M	V_M Pin Input Voltage	$V_{DD} - 28$ to $V_{DD} + 0.3$	V
V_{Co}	Co Pin Output Voltage	$V_{DD} - 28$ to $V_{DD} + 0.3$	V
V_{Do}	Do Pin Output Voltage	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
P_d	Power Dissipation	150	mW
T_{opt}	Operating Temperature Range	-40 to 85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$

Caution: These values must not be exceeded under any conditions.

Function Description

Normal Condition:

VDD is between the Overdischarge Detection voltage (Vdet2) and Overcharge Detection voltage (Vdet1) and the VM pad voltage is between Charger Detection Voltage (Vcha) and the Discharge Overcurrent Detection voltage (Vdet3), therefore the outputs of D_O pad and C_O pad are high and the MOSFETs of charge and discharge are all on. Charging and discharging can be carried out freely.

Overcharge Condition:

When VDD increases and passes Vdet1 during charging under the normal condition, the output of Co pad will change from high to low after Overcharge Detection Delay Time (Tvdet1), turning off the charging control FET.

If, within Tvdet1, VDD becomes lower than Vdet1 and stays for duration shorter than Overcharge Reset Delay Time (Treset) before rising up over Vdet1 again, this type of instantaneous falling of VDD is ignored. Otherwise, if the time VDD stays lower than Vdet1 is longer than Treset, the timing related to Tvdet1 shall be reset.

Charge Overcurrent Condition:

If the VM pin voltage falls below the Charger Detection Voltage (Vcha) during charging under normal condition and it continues for the Charge Overcurrent Delay Time (Tab) or longer, the charging control FET turns off and charging stops. This action is called the Charge Overcurrent detection.

Charge Overcurrent detection works when the D_O pin voltage is "H" and the VM pin voltage falls below the Charger Detection Voltage (Vcha). To an overdischarged battery, only when charging makes the battery voltage higher than the Overdischarge Detection voltage (Vdet2), the Charge Overcurrent Detection can act. Charge overcurrent state is released, once the voltage difference between VM pin and VSS pin becomes less than the Charge Overcurrent Detection voltage (Vcha) value.

Overcharge Protection Release Condition:

The charging state can be reset and charge control FET will turn on, as follow condition:

- (1) When the VM voltage is equal to or higher than Vdet3 (eg.when a charger is disconnected and a load is connected), VDD becomes lower than the Overcharge Detection Voltage (Vdet1), and stays longer than Overcharge Release Delay Time (Tvrel1), the charge control FET turns on.
- (2) When the VM voltage is between Vdet3 and Vcha (usually only be forced intentionally), VDD becomes lower than the Overcharge Release Voltage (Vrel1), and stays longer than Overcharge Release Delay Time (Tvrel1), the charge control FET turns on.
- (3) When the VM voltage is lower than Vcha (eg.when a charger is connected), even if VDD level is lower than Vrel1, the overcharge state will not release and charge control FET keep off until disconnect the charger with the battery pack.

Note1: when a charger is disconnected and a load is connected, the VM voltage is pulled to a value higher than Vdet3. Then IC detects the load-connecting condition.

Note2: when a charger keeps connecting, the VM voltage is equal to the voltage difference between VDD and charger which is lower than Vcha.

Overdischarge Condition:

While discharging, after VDD lowers below Overdischarge Detection voltage (Vdet2), Do pad goes low after Overdischarge Detection Delay Time (Tvdet2). The Do pad would switch off the discharging control FET and stop discharging.

Overdischarge Protection Release Condition:

When IC is in overdischarge condition, if a charger is connected to the battery pack, and the battery supply voltage becomes higher than V_{det2} , and V_M is lower than Charger Detection Voltage (V_{cha}), Do pad becomes high, allowing discharging action.

The discharging state also can be reset and the output of Do becomes high when VDD becomes higher than the Overdischarge Release Voltage (V_{rel2}), V_M is between V_{det3} and V_{cha} , stays longer than Release Delay Time (T_{vrel2}).

When a charger is connected from the battery pack, while the VDD level is lower than V_{det2} , the battery pack makes charger current allowable through the internal parasitic diode.

Charger Detect Condition:

When a battery in the overdischarge condition is connected to a charger and provided that the V_M pin voltage is lower than the Charger Detection Voltage (V_{cha}), IC releases the overdischarge condition and turns on the discharging control FET as the battery voltage becomes higher than the Overdischarge Detection Voltage (V_{det2}) since the charger detection function works. This action is called charger detection.

When a battery in the overdischarge condition is connected to a charger and provided that the V_M pin voltage is between the Charger Detection Voltage (V_{cha}) and overcurrent

Detection voltage (V_{det3}), IC releases the Overdischarge condition when the battery voltage reaches the Overdischarge Release Voltage (V_{rel2}) or higher.

Discharge Overcurrent Protection:

During discharging, the current varies with load, and V_M increases with the rise of the discharging current. Once V_M rises up to the Discharge Overcurrent Detection voltage (V_{det3}) or higher and stays longer than the Discharge Overcurrent Delay Time (T_{vdet3}), Do pad switches to low, turning off the discharging control FET. After that Discharge Overcurrent state is removed, i.e. $V_M < V_{riov}$, and the circuit recovers to normal condition.

Short Circuit Protection:

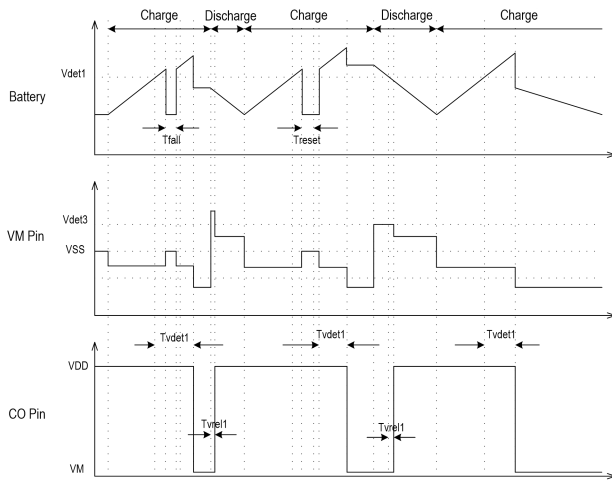
This function has the same principle as the overcurrent protection. But, the delay time T_{short} is far shorter than T_{vdet3} , and the detection voltage V_{short} is far higher than V_{det3} . When the circuit is shorted, V_M increases rapidly. Once $V_M \geq V_{short}$, Do pad switches to low, turning off the discharging control FET. After the short circuit state is removed, i.e. $V_M < V_{riov}$, the circuit recovers to the normal condition. The short circuit peak current is related to V_{short} and the ON resistance of the two FETs in series. Output types of Co and Do are CMOS level.

0V battery charge function

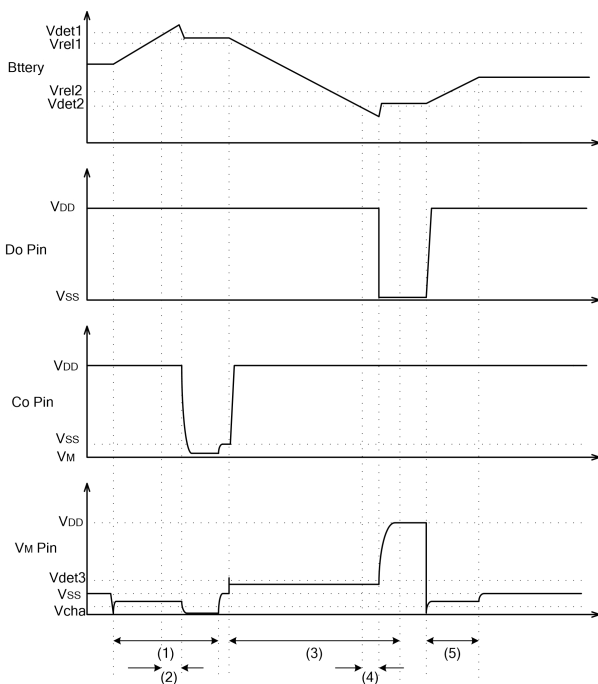
This function is used to recharge the connected battery whose voltage is 0V due to the self-discharge. When the 0 V battery charge starting charger voltage (V_{0cha}) or higher is applied between P+ and P- pins (see the Typical Application Circuits of Page1) by connecting a charger, the charging control FET gate is fixed to VDD pin voltage. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging control FET turns on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than the Overdischarge Detection voltage (V_{det2}), the IC enters the normal condition.

Operation Timing Chart

Operation Timing Chart (1) Overcharge, Timer Reset for Overcharge

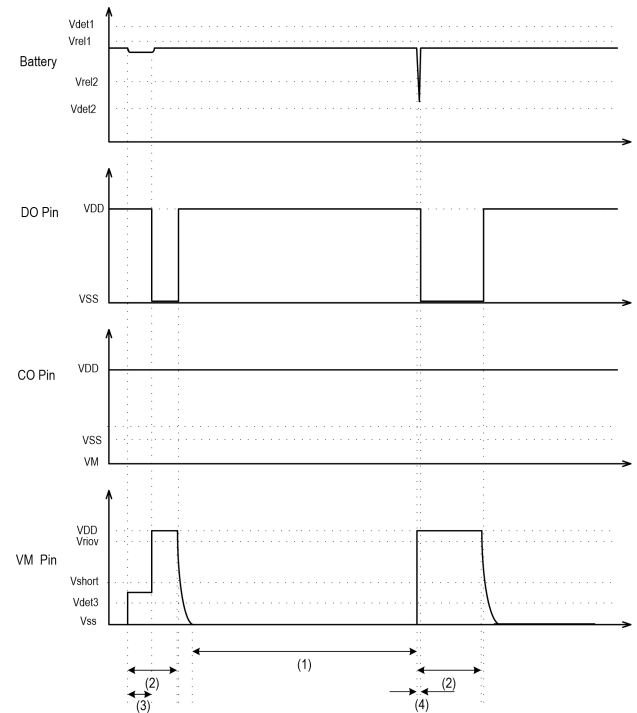


Operation Timing Chart (2) Overcharge/Overdischarge Detection



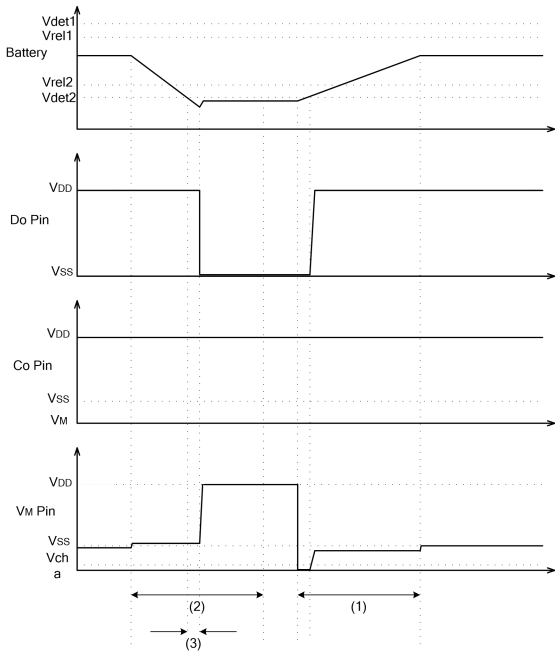
- (1) Charger connected
- (2) Overcharge Detection Delay Time (T_{vdet1})
- (3) Load connected
- (4) Overdischarge Detection Delay Time (T_{vdet2})
- (5) Normal charging

Operation Timing Chart (3) Discharge Overcurrent and Short Protection



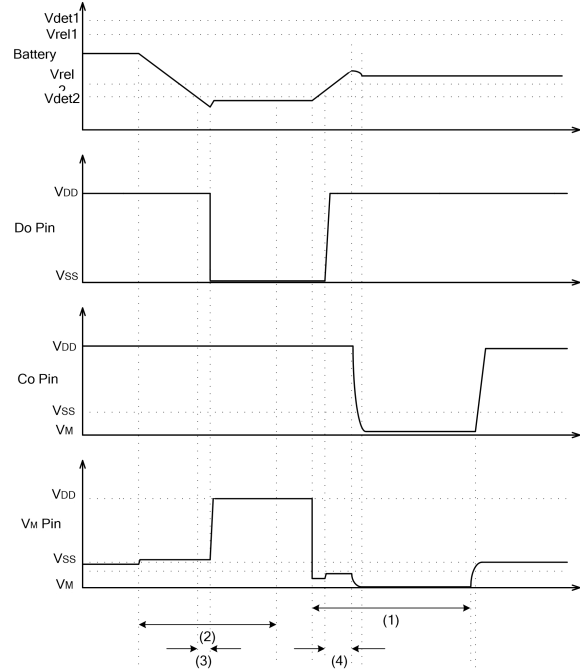
- (1) Normal condition
- (2) Load connection
- (3) Discharge Overcurrent Delay Time (T_{vdet3})
- (4) Short Circuit Delay Time (T_{short})

Operation Timing Chart (4) Charger Connection Detection



- (1) Charger connection
- (2) Load connection
- (3) Overdischarge Detection Delay (T_{vdet2})

Operation Timing Chart (5) Charge Overcurrent Detection



- (1) Charger connection
- (2) Load connection
- (3) Overdischarge Detection Delay Time (T_{vdet2})
- (4) Charging Overcurrent Detection Delay Time

Test Circuits

(1) Overcharge detection voltage and overcharge release voltage (Test circuit 1)

The Overcharge Detection Voltage (V_{det1}) is the voltage between V_{DD} and V_{SS} to which when V_1 increases and keeps the condition for overcharge delay time, V_{CO} changes from "H" to "L". The Overcharge Release Voltage (V_{rel1}) is the voltage between V_{DD} and V_{SS} to which when V_1 decreases, V_{CO} changes from "L" to "H".

(2) Overdischarge detection voltage and over-discharge release voltage (Test circuit 1)

The Overdischarge Detection Voltage (V_{det2}) is the voltage between V_{DD} and V_{SS} to which when V_1 decreases and keep the condition for overdischarge delay time, V_{DO} changes from "H" to "L". The overdischarge Release Voltage (V_{rel2}) is the voltage between V_{DD} and V_{SS} to which when V_1 increases, V_{DO} changes from "L" to "H".

(3) Discharge Overcurrent detection voltage and short circuit detection voltage (Test circuit 2)

The Discharge Overcurrent Detection Voltage (V_{det3}) is the voltage between V_M and V_{SS} to which when V_M increases within 10 us and keep the condition for Discharge Overcurrent Delay Time (T_{vdet3}), V_{DO} changes from "H" to "L".

The Short Circuit Detection Voltage (V_{short}) is the voltage between V_M and V_{SS} to which when V_M increases within 10us and keep the condition for Short Circuit Delay Time (T_{short}), V_{DO} changes from "H" to "L".

(4) Charger detection voltage and charge overcurrent detection voltage (Test circuit 2)

In the overdischarge condition, increase V_1 gradually until it is between V_{det2} and V_{rel2} . The voltage between V_M and V_{SS} to which when V_2 decreases, V_{DO} changes from "L" to "H", is the Charger Detection Voltage (V_{cha}).

In the normal charging condition, the voltage between V_M and V_{SS} to which when V_2 decreases, V_{CO} changes from "H" to "L" is the charge overcurrent detection voltage. It has the same value as the Charger Detection Voltage (V_{cha}).

(5) 0V battery charge starting charger voltage (Test circuit 2)

Set $V_1=V_2=0V$ and decrease V_2 gradually. The voltage between V_{DD} and V_M when V_{CO} goes "H" ($V_{VM}+0.1V$ or higher) is the 0V battery charge starting charger voltage.

(6) Normal operation current consumption and power down current consumption (Test circuit 2)

Set $V_1=3.5V$ and $V_2=0V$ under normal condition, the current I_{DD} flowing through V_{DD} pin is the normal operation consumption current (I_{DD}).

Set $V_1=3.5V$ and $V_2=0V$, let IC work in normal condition, set V_1 from 3.5V to 2.0V, then let V_M floating under overdischarge condition, the current I_{DD} flowing through V_{DD} pin is the power down current consumption ($I_{STANDBY}$).

(7) Overcharge detection (release) delay time and overdischarge detection (release) delay time (Test circuit 3)

If V_1 increases to be V_{det1} or over V_{det1} and keeps the condition for some time, V_{CO} will change from "H" to "L".

The time is called overcharge detection delay time. It is used to judge whether overcharge happens indeed. If V_1 decreases from V_{det1} or over V_{det1} to below V_{rel1} , V_{CO} will change from "L" to "H". The difference between this time and T_{reset} is called overcharge release delay time.

If V_1 decreases to be V_{det2} or below V_{det2} and keeps the condition for some time, V_{DO} will change from "H" to "L".

The time is called overdischarge detection delay time. It is used to judge whether overdischarge happens indeed. If V_1 increases from V_{det2} or below V_{det2} to over V_{rel2} and keeps the condition for some time, V_{DO} will change from "L" to "H". The time is called overdischarge release delay time.

(8) Discharge Overcurrent detection delay time and short circuit detection delay time (Test circuit 3)

If V2 increases to be Vdet3 or over Vdet3 and keeps the condition for some time, V_{DO} will change from “H” to “L”. The time is called Discharge Overcurrent delay time. It is used to judge whether Discharge Overcurrent happens indeed.

If V2 increases to be Vshort or over Vshort and keeps the condition for some time, V_{DO} will change from “H” to “L”. The time is called short circuit delay time. It is used to judge whether short circuit happens indeed.

(9) Co pin H resistance, Co pin L resistance (Test circuit 4)

Set V1=3.9V, V2=0 V, I_{co}=50uA (from Co to V3), K1 on and K2 off. (V1-V3)/I_{co} is the Co pin H resistance.

Set V1=4.5 V, V2=0 V, I_{co}=-50uA (from V3 to Co), K1 on and K2 off. V3/I_{co} is the Co pin L resistance.

(10) Do pin H resistance, Do pin L resistance (Test circuit 4)

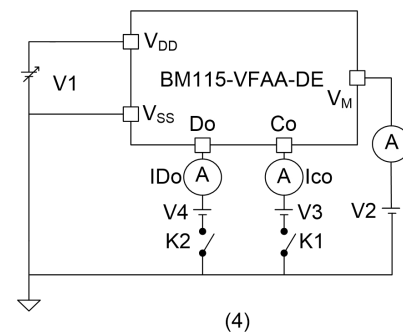
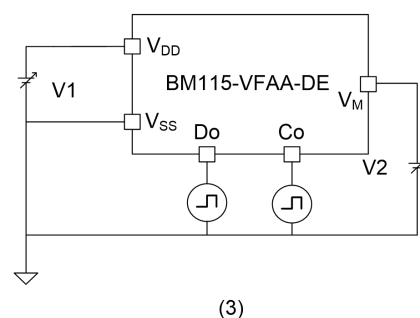
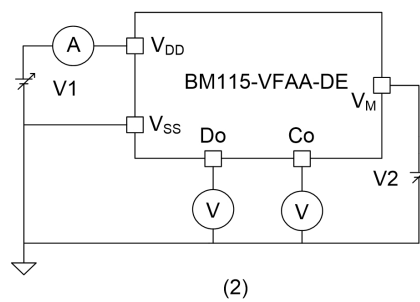
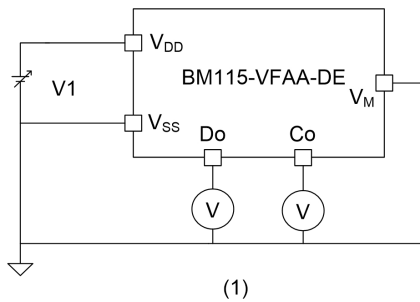
Set V1=3.9 V, V2=0 V, I_{Do}=50uA (from Do to V4), K1 off and K2 on. (V1-V4)/I_{Do} is the Do pin H resistance.

Set V1=2.0 V, V2=0 V and I_{Do}=50uA (from V4 toDo), K1 off and K2 on. V4/I_{Do} is the Do pin L resistance.

(11) Internal resistance VM -VDD and VM -VSS (Test circuit 4)

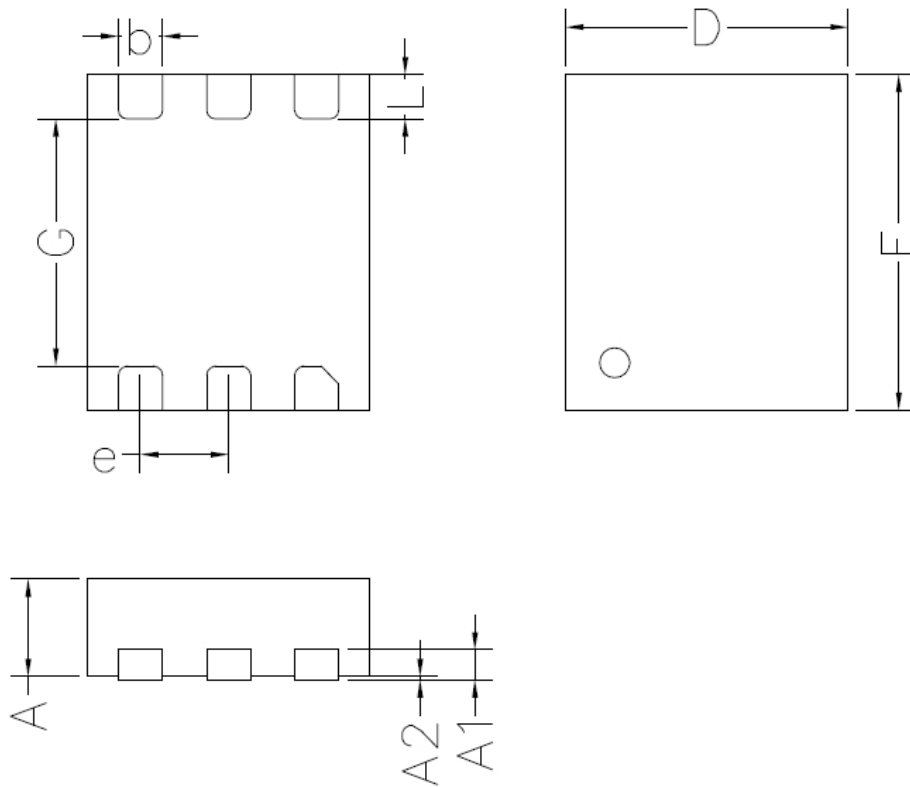
Set V1=2.0 V, V2=0 V, K1 off and K2 off, V1/I_{VM} is the internal resistance R_{VM}D.

Set V1=3.3 V, V2=1 V, K1 off and K2 off, V2/I_{VM} is the internal resistance R_{VM}S.



Package Outline

DFN 1.6×1.9-6L



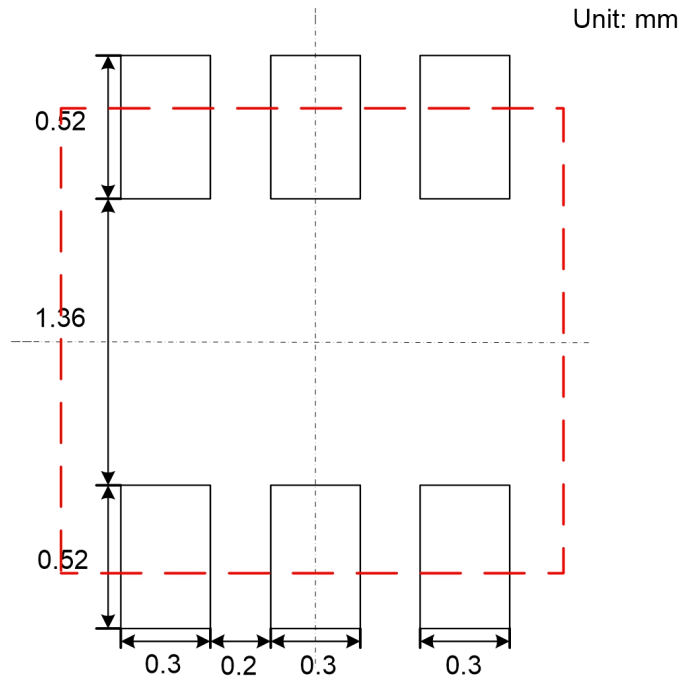
unit:mm

	MIN	NOM	MAX
D	1.55	1.60	1.65
E	1.85	1.90	1.95
L	0.20	0.25	0.30
b	0.20	0.25	0.30
e	0.5BSC		
G	1.400REF		
A	0.45	0.50	0.55
A1	0.15REF		
A2	0.00	0.02	0.05

Packing

MBB packing.7"reel: 3000pcs per reel.

PCB Layout





RESTRICTIONS ON PRODUCT USE

- The information contained herein is subject to change without notice.
- BYD Semiconductor Company Limited exerts the greatest possible effort to ensure high quality and reliability. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing products, to comply with the standards of safety in making a safe design for the entire system, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue. In developing your designs, please ensure that products are used within specified operating ranges as set forth in the most recent products specifications.
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